



UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ Fee Transmittal Form
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3. ☒ Drawing(s) (35 USC 113) Total Sheets
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[Note Box 5 below]
- i. ☐ DELETION OF INVENTOR(S)
Signed Statement attached deleting
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8. ☐ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney
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CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS (37 CFR 1.16(c))	32-20 =	12	X \$ 18.00 =	\$ 216.00
	INDEPENDENT CLAIMS (37 cfr 1.16(b))	2-3 =	0	X \$ 78.00 =	\$ -0-
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d))			\$260.00 =	\$ -0-
				BASIC FEE (37 CFR 1.16(a))	\$760.00
			Total of above Calculations =		\$976.00
	Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).				
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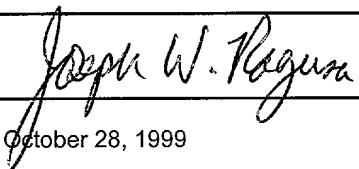
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED	
NAME	Joseph W. Ragusa (38,586)
SIGNATURE	
DATE	October 28, 1999

SOLID-STATE IMAGE PICKUP DEVICE AND METHOD OF
RESETTING THE SAME

BACKGROUND OF THE INVENTION

5 Field of the Invention

This invention relates to a solid-state image pickup device to be used for an image input apparatus such as a digital camera, a video camera, an image scanner or an AF sensor and also to a method of
10 resetting the same.

Related Background Art

Typical examples of solid-state image pickup device include the CCD image sensor and the non-CCD image sensor. The former comprises a photoelectric
15 converter having photodiodes and a CCD shift register, whereas the latter comprises a photoelectric converter having photodiodes or photo-transistors and a scanning circuit having MOS transistors.

The APS (active pixel sensor) is a type of non-CCD
20 image sensor comprising a photodiode and MOS transistors.

More specifically, an APS comprises combinations of a photodiode, a MOS switch and an amplifier for amplifying the signal from the photodiode, each
25 combination being arranged in correspondence to a pixel, and provides a number of advantages including the capabilities of "XY addressing" and "realizing the

sensor and the signal processing circuit in a single chip". On the other hand, it is rather difficult for an APS to reduce the chip size that is a determinant of the dimensions of its optical system because of the large number of elements it has for each pixel. This is the reason why the market for solid-state image pickup devices has been dominated by conventional CCD image sensors to date.

However, in recent years, due to the technological development for miniaturizing MOS transistors and the strong demand for "realizing the sensor and the signal processing circuit in a single chip" and "reducing the power consumption rate of the image sensor for the purpose of power saving", the APS has been attracting attention as it is also called a CMOS sensor.

FIG. 23 of the accompanying drawings schematically illustrates the pixel section of a known APS and its operation.

Referring to FIG. 23, photoelectric converter PD is a buried type photodiode similar to the one typically used in a CCD. With a buried type photodiode, the dark current that can be generated on the SiO_2 surface can be suppressed by arranging a p^+ -layer containing an impurity to a high concentration level on the surface and the saturation charge of the photodiode can be raised by the junction capacitance generated between the n-layer of the storage portion

and the p⁺-layer of the surface. It operates in a manner as described below. Firstly, diffusion region FD is reset to a reference voltage by applying an on-pulse to gate RST. Thereafter, an off-pulse is applied to the gate RST to bring the diffusion region into a floating state in order to start storing data. After a certain period of time, another on-pulse is applied to gate TX to read the charge of the optical signal stored in the photoelectric converter PD to floating diffusion region FD, which is the input terminal of the amplifier of the APS, by way of MOS transfer section TX. Then, the signal charge Q_{sig} is converted into voltage Q_{sig}/C_{FD} by means of the capacitance C_{FD} of the floating diffusion region FD and the signal is read by way of a source-follower circuit that uses the floating diffusion region FD as its input terminal.

When a reverse bias voltage is applied to a buried type photodiode, depletion layers extend from the PN junction at the interface with the surface p⁺-layer and from the PN junction at the interface with the P-type well PWL perpendicularly into the n-layer. At this time, the number of electrons in the n-layer of the photodiode is substantially equal to that of the neutral region located between the two depletion layers and it is reduced in proportion to the width of the depletion layers. The number of electrons of said neutral region when the reverse bias voltage is 0 volt

corresponds to the saturation charge Q_{sat} . As the both depletion layers extend to contact each other by the reverse bias voltage, the inside of the photodiode is completely depleted to make the neutral region non-existent. The reverse bias voltage for making the neutral region non-existent will be referred to as depletion voltage V_{dp} in the following description.

If a reverse bias voltage greater than the depletion voltage is applied, the electron concentration of the n-layer of the photodiode decreases as an exponential function of the reverse bias voltage.

When the n-layer of the photodiode of an APS having a configuration as described above is depleted, the electric charge generated by light is almost totally transferred to the floating diffusion region FD to reset the electron state in the photodiode. A mode of transferring almost all the electric charge of the photodiode is referred to as depletion transfer hereinafter.

FIG. 24 of the accompanying drawings shows the relationship between the saturation charge of a photodiode and the voltage of the floating diffusion region FD upon reading the saturation charge and also the relationship between the saturation charge of the photodiode and the depletion voltage Z . Then, the voltage V_{FDsat} of the floating diffusion region FD is

expressed by the formula below:

$$V_{FDsat} = V_{res} - Q_{sat}/C_{FD}$$

where V_{res} is the reset voltage, Q_{sat} is the saturation charge of the photodiode and C_{FD} is the capacitance of the floating diffusion region.

Generally, the saturation charge of a photodiode has to be higher than the level of realizing a desired sensitivity, which may be A in FIG. 24. For realizing a depletion transfer, on the other hand, the requirement of

$$V_{FDsat} > V_{dp}$$

has to be met, provided that V_{dp} is the depletion voltage of the photodiode, which is indicated by B in FIG. 24. If $V_{FDsat} < V_{dp}$, the reverse bias voltage of the photodiode will become the voltage of the floating diffusion region to leave a neutral region within the photodiode and hence the signal voltage will be read out in accordance with the capacitance division between the capacitance attributable to the both depletion layers and the capacitance of the floating diffusion region. At the same time, electrons will remain in the photodiode by an amount equal to the saturation charge Q_{sat} after the reading operation so that they can give rise to a residual image and a noise.

As described above, in the known APS, the saturation charge Q_{sat} of the photodiode is made to meet the requirement of $A < Q_{sat} < B$ so as to be found within

the interval of C in FIG. 24.

However, the saturation charge Q_{sat} or the depletion voltage V_{dp} is apt to be affected by variances of the manufacturing process. For instance, the depletion voltage can be shifted by 0.4 volt when the dose of ion implantation for forming the n-layer of the photodiode is varied by 10%.

Then, the net result is a low manufacturing yield.

10 SUMMARY OF THE INVENTION

Therefore, it is an object of the present invention to provide a solid-state image pickup device that can effectively reduce the residual charge in the photoelectric converter and operate effectively and efficiently for photoelectric conversion and also a method of resetting the same.

Another object of the present invention is to expand the process tolerance for manufacturing a solid-state image pickup device that is adapted to be reset in a desired manner.

According to the invention, the above objects and other objects of the invention are achieved by providing a solid-state image pickup device comprising a photoelectric converter, an input terminal for signal amplifier, a transfer switch for transferring an electric charge from the photoelectric converter to the input terminal and a reset switch for applying a reset

voltage to the input terminal, wherein said device is adapted to input a pulse signal to the reset switch and the transfer switch in order to turn on said reset switch and said transfer switch simultaneously.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic circuit diagram of a preferred embodiment of solid-state image pickup device according to the invention.

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FIG. 2 is a drive timing chart illustrating the operation of the preferred embodiment of solid-state image pickup device according to the invention.

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FIG. 3 is a schematic cross sectional view of a principal portion of the preferred embodiment of solid-state image pickup device according to the invention.

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FIG. 4 is a schematic illustration of changes that can take place in the potential profiles of principal sections of the preferred embodiment of solid-state image pickup device according to the invention.

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FIG. 5 is a graph showing the dependency of the voltage of the floating diffusion region on the saturation charge, illustrating the reset voltage necessary for depleting the photoelectric converter of the preferred embodiment of solid-state image pickup device according to the invention.

FIG. 6 is a schematic cross sectional view of a principal portion of another preferred embodiment of

solid-state image pickup device according to the invention.

FIG. 7 is a schematic illustration of changes that can take place in the potential profiles of principal sections of the preferred embodiment of solid-state
5 image pickup device according to the invention.

FIG. 8 is a drive timing chart illustrating the operation of the preferred embodiment of solid-state image pickup device according to the invention.

10 FIG. 9 is a schematic circuit diagram of a pixel of still another preferred embodiment of solid-state image pickup device according to the invention.

FIG. 10 is a schematic circuit diagram of the preferred embodiment of solid-state image pickup device
15 according to the invention.

FIG. 11 is a drive timing chart illustrating the operation of the preferred embodiment of solid-state image pickup device according to the invention.

FIG. 12 is another drive timing chart that can be
20 used for the operation of the preferred embodiment of solid-state image pickup device according to the invention.

FIG. 13 is a schematic illustration of an image input apparatus that can be realized by using a solid-
25 state image pickup device according to the invention.

FIG. 14 is a drive timing chart illustrating the operation of the image input apparatus.

FIG. 15 is a schematic circuit diagram of still another preferred embodiment of solid-state image pickup device according to the invention.

FIG. 16 is a drive timing chart illustrating the operation of the preferred embodiment of solid-state image pickup device according to the invention.

FIG. 17 is a schematic circuit diagram of still another preferred embodiment of solid-state image pickup device according to the invention.

FIG. 18 is a drive timing chart illustrating the operation of the preferred embodiment of solid-state image pickup device according to the invention.

FIG. 19 is another drive timing chart that can be used for the operation of the preferred embodiment of solid-state image pickup device according to the invention.

FIG. 20 is a graph illustrating the dependency of the output of the preferred embodiment of solid-state image pickup device according to the invention on the quantity of incident light.

FIG. 21 is a schematic cross sectional view of a principal portion of the preferred embodiment of solid-state image pickup device according to the invention.

FIG. 22 is a schematic illustration of changes that can take place in the potential profiles of principal sections of the preferred embodiment of solid-state image pickup device according to the

invention.

FIG. 23 is a schematic cross sectional view of the preferred embodiment of solid-state image pickup device according to the invention, illustrating a depletion transfer thereof.

FIG. 24 is a graph illustrating the dependency of the voltage necessary for depletion transfer on the saturation charge of the preferred embodiment of solid-state image pickup device according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, the present invention will be described in greater detail by referring to the accompanying drawings that illustrate preferred embodiments of the invention.

Embodiment 1

FIG. 1 is a schematic circuit diagram of a pixel of a preferred embodiment of solid-state image pickup device according to the invention and FIG. 2 is a drive timing chart illustrating the operation of the preferred embodiment of solid-state image pickup device according to the invention. Note that the basic configuration of this embodiment is commonly applicable to the remaining embodiments as will be described hereinafter.

The photoelectric converter PD typically comprises a photodiode having a PN junction or a PIN junction.

One of the terminals of the photoelectric converter is held to a reference potential for applying a reverse bias voltage, while the other terminal thereof is connected to a transfer switch Q1. From FIG. 1, it will be seen that the cathode is connected to the transfer switch Q1 to transfer electrons.

In FIG. 1, Q2 denotes a reset switch having one of its terminals connected to reference voltage source VDD for applying a resetting voltage.

Q3 denotes a transistor operating as amplifier for outputting a signal obtained by amplifying the signal input to the gate that operates as input terminal.

Q4 denotes a selection switch for selecting a pixel from which a signal is to be read out.

A pulse signal as shown in FIG. 2 is applied to the gate of each of the switches from a control circuit SCC.

FIG. 3 is a schematic cross sectional view of the semiconductor chip incorporating part of the circuit of FIG. 1 and FIG. 4 is a schematic illustration of changes that can take place in the potential profiles of principal sections of the embodiment. In FIGS. 3 and 4, TX denotes the potential energy under the gate of the transfer switch and RST denotes the potential energy under the gate of the reset switch.

The n-type semiconductor layer of the photoelectric converter PD is held in common with one

of the main electrodes of the MOS transistor of the transfer switch Q1 and the other main electrode of the transfer switch Q1 also operates as floating diffusion region FD, which will operate as input terminal of the amplifier.

The reset switch Q2 comprises a MOS transistor having a pair of main electrodes, which are the floating diffusion region FD and the semiconductor region to which the reference voltage VDD is applied for resetting.

The floating diffusion region FD is connected to the gate of the transistor Q3, although the transistors Q3 and the selection switch Q4 are not shown in FIG. 3.

FIG. 2 and FIG. 4 illustrate how the embodiment of FIG. 1 operates. Firstly, the diffusion region FD is reset to the reference voltage by inputting a high level pulse such as ϕ_{RST} to the gate of the reset switch Q2. P1 in FIG. 4 shows the potential profile that will be observed at this time.

Then, the photoelectric converter PD is reset by inputting a high level pulse such as ϕ_{TX} to the gate of the transfer switch Q1. Since the reset switch Q2 is held on at this time, the potential profile will be such as the one indicated by P2 at this time so that the electric charge will be completely transferred to the diffusion region FD.

Subsequently, the transfer switch Q1 is turned off

to isolate the photoelectric converter PD and the diffusion region FD from each other. Then, since any residual electric charge of the photoelectric converter PD has been completely transferred to the diffusion region FD, the n-layer of the photoelectric converter PD will be completely depleted.

As the transfer switch Q1 is turned off, the photoelectric converter PD starts storing a photoelectric charge.

10 Thereafter, the reset switch Q2 is turned off. Then, the potential profile will be such as the one indicated by P3 in FIG. 4.

After storing the electric charge for a certain period of time, the transfer switch Q1 is turned on once again to transfer the electric charge stored in the photoelectric converter to the floating diffusion region FD. P4 in FIG. 4 indicates the potential profile that will be observed at this time.

20 Then, after turning off the transfer switch Q1, selection pulse ϕ_T is input to the gate of the selection switch Q4 and the signal amplified by the transistor Q3 is read out.

P5 in FIG. 4 indicates the potential profile that will be observed after turning off the transfer switch Q1.

Any residual electric charge remaining in the photoelectric converter PD will be removed by carrying

out the above resetting operation for another time.

In this embodiment, a reverse bias voltage higher than the depletion voltage is selected as reference voltage VDD to be used for resetting operations and the transfer switch Q1 is turned on while applying this voltage to the diffusion region FD by way of the reset switch Q2.

In this way, a reverse bias voltage higher than the depletion voltage is applied to the photodiode to sufficiently reduce the residual electric charge in the photodiode. If the saturation charge Q_{sat} of the photodiode is found between B and F in FIG. 5 and the transfer switch of the prior art is turned on while an electric charge corresponding to the saturation charge is stored in the photodiode, a large electric charge exists in the photodiode because $V_{FDsat} < V_{dp}$. If the transfer switch Q1 is turned off to enter the next storage period and the signal charge is read out under this condition, the residual electric charge that is not read out in the last reading period will be added to the signal charge read out this time.

To the contrary, according to the invention, the electric potential of the diffusion region FD is held to a level that is sufficiently high for applying a reverse bias voltage higher than the depletion voltage V_{dp} to the photodiode and then any electric charge remaining in the photodiode is eliminated to reset the

latter by turning on the transfer switch.

As a result, no depletion transfer operation is required for the electric charge of the photodiode at the time of signal transfer so that, unlike the prior art, no problem of residual image occurs under the condition of

$$V_{\text{FDsat}} = V_{\text{res1}} - Q_{\text{sat}}/C_{\text{FD}} < V_{\text{dp}}.$$

Therefore, the saturation charge Q_{sat} of the photodiode only has to meet the requirement of $A < Q_{\text{sat}} < F$. This means that a greater tolerance is allowed for variances in designing and manufacturing photodiodes and hence the manufacturing yield will be improved.

Meanwhile, the margin of the saturation charge Q_{sat} for realizing $V_{\text{FDsat}} > V_{\text{dp}}$ may be widened by raising the reset voltage V_{res} . In other words, the margin of the saturation charge Q_{sat} can be widened from interval AB to interval AE by raising the reset voltage V_{res} of the floating diffusion region from V_{res1} to V_{res2} in FIG. 5.

Then, however, the supply voltage has to be raised at least by more than 5 volt. This entails a higher power consumption rate and the need of arranging an additional power source for the sensor chip along with other problems that can degrade the performance of the chip.

Embodiment 2

Now, another embodiment of the present invention

will be described by referring to FIGS. 6, 7 and 8.

FIG. 6 is a schematic cross sectional view of the second embodiment of solid-state image pickup device according to the invention. FIG. 7 is a schematic illustration of changes that can take place in the potential profiles of principal sections of the embodiment of solid-state image pickup device of FIG. 6. FIG. 8 is a drive timing chart illustrating the operation of the preferred embodiment of solid-state image pickup device of FIG. 6. Note that the embodiment of solid-state image pickup device of FIG. 6 has a basic circuit configuration same as the embodiment of FIG. 1.

Referring to FIG. 6, the photodiode of the photoelectric converter of this embodiment is a buried type photodiode comprising a P-type well 101 formed in the substrate surface, a N-type region 105 and a surface p-region 104. As described above, with a buried type photodiode, the dark current that can be generated at the interface with the oxide film 106 of SiO_2 can be suppressed by arranging a p^+ -layer containing an impurity to a high concentration level at the surface. Additionally, the saturation charge of the photodiode can be raised by the junction capacitance generated between the n-layer of the storage section and the p^+ -layer of the surface. In FIG. 6, there are also shown the gate electrode 102 of

transfer switch Q1, an n-type semiconductor region 103 which will operate as floating diffusion region FD and the gate electrode 107 of reset switch Q2.

FIG. 7 illustrates changes of potential profile, and PD denotes the photodiode, while TX denotes the portion under the gate of the transfer switch and RST denotes the portion under the gate of the reset switch.

The embodiment of solid-state image pickup device operates in a manner as described below.

Referring to FIG. 8, after the photodiode and the floating diffusion region 103 are reset, the noise is read out from output terminal Vout by means of a read circuit as shown in FIG. 1.

Then, as shown in FIG. 8, the transfer switch Q1 is turned on by applying a high level signal (transfer signal ϕ_{TX}) to the gate 102 of the transfer switch Q1 and the optical signal charge stored in the photodiode is read out to the floating diffusion region 103 (FD) by way of the transfer switch. PP1 in FIG. 7 shows the potential profile that will be observed at this time.

Then, as shown in FIG. 8, the transfer switch Q1 is turned off by applying a low level signal to the gate 102 of the transfer switch Q1 and the sensor signal is read out by applying a read signal to a source follower circuit. The sensor signal is read out by transforming the signal charge Q_{sig} into voltage Q_{sig}/C_{FD} by means of the capacitance C_{FD} of the floating

diffusion region FD. PP2 in FIG. 7 shows the potential profile that will be observed at this time.

Then, the reset switch Q2 is turned on by applying a high level signal (reset signal ϕ_{RST}) to the reset switch Q2 in order to reset the floating diffusion region 103 as shown in FIG. 8. Additionally, the transfer switch Q1 is also turned on to reset the photodiode. PP3 in FIG. 7 shows the potential profile that will be observed at this time.

Then, after turning off the transfer switch Q1, the reset switch Q2 is also turned off to terminate the resetting operation. PP4 in FIG. 7 shows the potential profile that will be observed after terminating the resetting operation.

As described above, a resetting operation can be carried out to deplete the photodiode prior to a storage operation without additionally arranging an overflow-drain element or a reset element for the photodiode, by holding the voltage of the floating diffusion region to a level that is sufficiently high for applying a reverse bias voltage higher than the depletion voltage to the photodiode before opening the transfer switch. Then, a greater tolerance is allowed for variances in manufacturing photodiodes and hence the manufacturing yield will be improved.

Embodiment 3

FIG. 9 is an equivalent circuit diagram of a pixel

of the solid-state image pickup device according to the invention. In FIG. 9, the photodiode PD is a buried type photodiode as in the case of the preceding embodiments. Otherwise, there are shown a MOS transistor Q1 operating as transfer switch for
5 transferring a photoelectric charge to floating diffusion region FD, a MOS transistor Q2 operating as reset switch for resetting the floating diffusion region FD, an input MOS transistor Q3 of a source
10 follower for outputting the voltage of the floating diffusion region FD and a MOS transistor Q4 operating as selection switch for selecting a pixel. The input MOS transistor Q3 of the source follower takes the role of a signal amplifier and the floating diffusion region
15 FD operates as the input terminal of this signal amplifier.

FIG. 10 is a schematic circuit diagram of a solid-state image pickup device comprising a matrix of 2×2 pixels PX, each having a circuit configuration as shown
20 in FIG. 9.

The pixels PX1 and PX2 of the first row have a common selection signal line 503 for receiving pulse signal $\phi T1$ as input from control circuit SCC. Similarly, the pixels PX3 and PX4 of the second row
25 have a common selection signal line 503 for receiving pulse signal $\phi T2$ as input from the control circuit SCC.

Additionally, the pixels PX1 and PX3 of the first

column have a common signal output line 504, which is connected to a load array 511 and a memory 512.

Similarly, the pixels PX2 and PX4 of the second column have a common signal output line 504, which is also
5 connected to the load array 511 and the memory 512.

The memory 512 has a capacitance for storing a noise component and a capacitance for storing a signal component and is adapted to store an output signal in these capacitances upon receiving a sampling pulse as

10 input. Reset lines 502 and transfer control lines 506 are connected to the control circuit SCC so as to input a pulse signal to all the pixels or on a row by row basis in order to turn on a target transistor.

The signal read out from the memory 512 is scanned
15 by scanning circuit 513, which may be a shift register, and output by way of output terminal SG.

FIG. 11 is a drive timing chart illustrating drive pulses to be used for reading a pixel.

Before starting a storing operation, the transfer
20 switch Q1 is turned on by inputting a pulse ϕ_{TX} to the corresponding transfer control line 506 as indicated by T1, while keeping the reset switch Q2 in an on-state, to reset and deplete the photodiode.

For instance, when the voltage VDD of the power
25 supply line 501 is 5 volts and the reset switch Q2 is on, the floating diffusion region is made to show a voltage of about 3.5 volts. The depletion voltage V_{dp}

of the photodiode under this condition will be about 2.5 volts. As the photodiode is reset, the inside of the photodiode will be depleted. The depleted condition of the photodiode can be evidenced by means
5 of a residual image experiment.

Subsequently, a signal is stored for 1/30 seconds. The reset switch Q2 is held on mostly during the signal storing period. Thereafter, the reset switch Q2 is turned off by applying a pulse as indicated by T3 to
10 bring the diffusion region FD into a floating state. Then, the selection switch Q4 is turned on to read out the stored signal by applying a pulse as indicated by T4. Thus, the voltage corresponding to the voltage of the floating diffusion region is output from the
15 corresponding signal output line 504 by means of the source follower comprising the load array 511 connected to the MOS transistor Q3 and the corresponding signal output line 504. This output is sampled by the memory 512.

20 In this instance, the noise component of the pixel can be read out by turning off the reset switch Q2 from an on-state and subsequently turning on the selection switch Q4 while keeping the transfer switch Q1 in an off-state during the reading period TR. For this
25 purpose, the noise component is stored in the noise storage capacitance of the memory 512 by means of a sampling pulse T5. After turning on the transfer

switch Q1 by means of a pulse T6, the signal component is stored in the signal storage capacitance of the memory 512 by applying a sampling pulse T7 also during the reading period.

5 Then, an output signal with a reduce noise level can be obtained by outputting the difference of the signal component and the noise component obtained in this way by means of a subtracter, which is typically a differential amplifier.

10 Since the diffusion region FD is in a floating state when sampling the signal component, the voltage V_{FD} of the diffusion region FD is expressed by subtracting Q/C_{FD} from the reset voltage V_{res} , or

15
$$V_{FD} = V_{res} - Q/C_{FD}$$
 (where Q is the transferred electric charge).

A signal corresponding to the voltage is output from the signal output line 504 and sampled.

20 Then, the inside of the photodiode is depleted before entering a subsequent storage period by turning on the reset switch Q2 and opening the transfer switch Q1 by means of a pulse T2.

25 In an experiment, the photoelectric conversion performance of the embodiment was evaluated by using the signal obtained as a result of the above operation to evidence a good linearity of the performance. The voltage of the floating diffusion region fell to 1.5 volts when the output was saturated.

For the purpose of comparison, the residual image was observed while constantly keeping the pulse ϕ_{TX} to the transfer switch Q1 at a low level to find a residual image of about 20 to 30%.

5 Table below summarily shows the obtained results.

	light	dark	
	1 st output	2 nd output	3 rd output
operation for comparison	2.0V	0.45V	0.2mV or less
10 operation of embodiment	2.0V	0.2mV or less	0.2mV or less

Embodiment 4

15 An operation of the embodiment of solid-state image pickup device as shown in FIG. 10 using another drive timing chart will be discussed below, although the reset phase of this operation is same as the above described one.

20 While FIG. 10 shows a matrix of 2×2 pixels, FIG. 12 shows a drive timing chart for the pixels of given three rows of a matrix having three or more than three rows.

25 In FIG. 12, each of the periods 7a, 7b and 7c correspond to the reading period TR in FIG. 11. On the other hand, periods 7A, 7B and 7C are horizontal scanning periods of sequentially outputting the signals of the respective rows stored in the memory 512 on a

time series basis by means of scanning circuit 513.

More specifically, in the reading period 7a, the signals of the pixels of the (n-1)-th row are read out and written in the line memory 512 for the row as the noise component and the optical signal component.

Then, in the horizontal scanning period 7A, the signals written in the line memory 512 are sequentially read out on a time series basis. All the photodiodes are storing signals at least during the horizontal scanning period 7A. Subsequently, the signals of the pixels of the n-th row are read out in the reading period 7b and the signals in the line memory 512 are read out in the horizontal scanning period 7B. Thus, the operation of reading out the signals from the pixels and then from the line memory is conducted on a row by row basis in a rolling shutter mode. As a result, an excellent moving image that is free from any residual image can be retrieved.

Embodiment 5

FIG. 13 is a schematic illustration of an image input apparatus realized by using a solid-state image pickup device 1 according to the invention. The apparatus comprises an optical system 3 such as a lens and a mechanical shutter 2 and the exposure time (storage time) of the solid-state image pickup device 1 is controlled by the shutter 2. The reset operation of the solid-state image pickup device 1 proceeds in a

manner as described above.

The image input apparatus operates in a manner as described below with referring to FIG. 14.

The photodiodes of the solid-state image pickup
5 device 1 are reset in the initial reset period 8s of
the overall open-shutter interval to eliminate all the
signals that may have been stored there. Then, signals
are stored and the shutter is closed after a
predetermined period of time. Then, the signals of the
10 pixels of the (n-1)-th row are read out to the line
memory 512 in the reading period 8b and subsequently
the signals held in the line memory 512 are
sequentially read out by means of the scanning circuit
513 in the horizontal scanning period 8B. Thereafter,
15 the signals of the pixels of the n-th row are read out
to the line memory in the reading period 8a and
subsequently the signals held in the line memory 512
are sequentially read out by means of the scanning
circuit 513 in the horizontal scanning period 8A. A
20 similar operation will be repeated to read out the
signals from the pixels of all the rows. This
technique is particularly adapted to picking up a still
image because all the pixels are provided with a same
and unique storage time.

25 Embodiment 6

FIG. 15 is a schematic illustration of a still
another embodiment of solid-state image pickup device

comprising a sensor section containing pixels arranged to form a matrix, a bus line for transmitting the signals from the sensor section to an A/D converter and a memory section for storing the A/D converted signals read out from all the pixels.

FIG. 16 is a drive timing chart illustrating the operation of the solid-state image pickup device of FIG. 15. The reset operation of the solid-state image pickup device 1 proceeds in a manner as described above.

Referring to FIG. 16, all the pixels are reset in the reset period 9s.

After a predetermined storage time, the mechanical shutter 2 is closed to terminate the operation of storing optical signals.

Then, in the reading period 9a, the signals of the (n-1)-th row are read out and input to the A/D converter by way of the bus line. Thus, the analog signals converted into digital signals, which are then written in the respective positions of the memory section having the predetermined respective addresses.

Subsequently, in the reading period 9b, the signals of the n-th row are read out, A/D converted and written in the respective positions of the memory section having the predetermined respective addresses.

Then, in the reading period 9c, the (n+1)-th row are read out and written in the respective positions of

the memory section having the predetermined respective addresses.

In this way, signals are stored after resetting all the photodiodes and the signals of each row are read out and input to the A/D converter by way of the bus line. Then, the image signals digitized by the A/D converter are written in the memory cells prepared for the respective pixels. Thus, the solid-state image pickup device according to the invention is adapted to pickup an image regardless if the image is a moving image or a still image. Particularly, in the case of a moving image, the immediately preceding image can be processed by means of a image processing IC during the storage period of the current image.

Embodiment 7

FIG. 17 is a schematic illustration of still another embodiment of solid-state image pickup device according to the invention.

The sensor section of this embodiment is divided into four blocks, which are provided with respective horizontal and vertical scanning selection circuits.

Each scanning selection circuit can be used to select a row and a column under the control of a scanning control IC with an independent timing.

The read out pixel signals are subjected to A/D conversion and the digitized signals are written in the memory section.

With this embodiment, the storage time of the current frame can be determined on a row by row basis according to the image signals of the immediately preceding frame.

5 For example, as shown in FIG. 18, the photodiodes are reset in the reset period 10S for the first frame and then a storage operation is started. Subsequently, signals are sequentially read out on a row by row basis in the reading periods 10a through 10c and written in
10 the memory section.

 If signals that can be regarded as saturated signals are found in the image signals stored in the memory section, the storage period of the next frame can be altered by shifting the timing of starting the
15 reset period.

 For example, when the reset period is started at a time for all the rows and some of the signals from the pixels of the n-th row and those from the pixels of the (n+1)-th row are saturated, the storage period of the
20 n-th row and the (n+1)-th row are shortened by forwardly shifting the reset periods 9Sn and 9Sn+1 on the basis of the judgment of the scanning control IC.

 In this embodiment, a relationship between the quantity of light and the sensor output as indicated by
25 C1 in FIG. 20 is obtained by controlling the storage period by means of the scanning control IC. More specifically, the operation of the photodiodes of this

embodiment is shifted forwardly from the end of the reset operation of the (n-1)-th row to reduce the storage period of the n-th row and that of the (n+1)-th row to about 1/2 of that of the (n-1)-th row. As a result, a phenomenon of saturated output that otherwise occurs as indicated by C2 in FIG. 20 if the reset period is started at a time for all the rows can be avoided and the output will show a curve C1, representing an excellent tone, even when the quantity of light entering the solid-state image pickup device is more than doubled from the ordinary level.

Embodiment 8

This embodiment is adapted to prevent the blooming phenomenon from taking place by holding the voltage applied to the transfer gate to a predetermined level so that the electric charge stored in the photodiodes during the storage period may partly flow out to the diffusion region FD that is held to the reset potential. FIG. 21 is a schematic cross sectional view of a principal portion of this embodiment of solid-state image pickup device.

For example, the potential barrier of the transfer gate TX is lowered slightly as indicated by S1 in FIG. 22 to make any excessive electric charge to flow into the diffusion region FD by raising the voltage of the low level pulse of ϕ_{TX} in FIG. 2 from the voltage of the P-type well 101.

To be more accurate, while the LOW level of the MOS transistor Q1 of the transfer switch shown in FIG. 2 or FIG. 11 is equal to the ground level, the LOW level of the MOS transistor Q1 of the embodiment is raised by 0.3 volt from the ground level. As a result, the potential profile of the photodiodes and the transfer switch will be like the one indicated by S1 in FIG. 22. Note that S2 in FIG. 22 indicates the corresponding potential profile when the LOW level is made equal to the GND level (0 volt).

In this embodiment, the low potential portion of the MOS transistor Q1 is made to operate as the channel section TX of the transfer switch and the transfer switch itself is made to operate as a horizontal type overflow drain by raising the LOW level of the MOS transistor Q1. In other words, the transfer switch is made to operate as a horizontal type overflow drain by holding the potential of the diffusion region to a fixed level during the storage period and controlling the gate voltage of the transfer switch so as to make it half open. As a result, any cross talk can be effectively suppressed.

As described above in detail, with any of the embodiments of the invention, the transfer switch can be opened by holding the floating diffusion region to a voltage level with which a reverse bias voltage higher than the depletion voltage can be applied before the

start of the next storage period. Thus, any residual electric charge remaining in the photoelectric converter can be eliminated to reset the latter so as to provide the advantages as listed below.

5 (1) Any transfer residue attributable to variances in the electric charge of the photodiodes that are brought in by the variances of the products can be eliminated after the transfer operation.

10 (2) A solid-state image pickup device that is free from any residual image can be provided without raising the power supply voltage and increasing the pixel size.

15 Meanwhile, Japanese Patent Publication No. 7-105915 described a method of resetting a photodiode by using a switch element arranged separately. However, the disclosed technique does not provide any appropriate way for reducing the pixel size.

20 With the technique disclosed in the above patent document, the photodiode is arranged within a well and shows a simple PN junction with a high concentration impurity region of the type opposite to that of the well. Such an arrangement, however, entails a large reset noise that is a function of the junction capacitance of the photodiode if the photodiode is reset. To the contrary, with a method of resetting a solid-state image pickup device according to the invention, the device is reset by depleting each of the photodiodes and the reset noise is, if any, negligible.

25

There are CCDs having an overflow drain function of using a vertical type overflow drain and a collective reset function of resetting all the pixels collectively. While such a device is adapted to
5 deplete the buried type photodiodes for resetting as in the case of a solid-state image pickup device according to the invention, a vertical type overflow drain has a device structure that is totally different from a surface device such as a MOS transistor and extends
10 downwardly. Therefore, although it does not occupy the pixel area, it cannot downwardly control the profile of the impurity. Additionally, such a device can only reset the pixels collectively.

To the contrary, with a solid-state image pickup
15 device according to the invention, the transfer switch can be made to operate as a horizontal type overflow drain by holding the potential of the diffusion region to a fixed level during the storage period and controlling the gate voltage of the transfer switch so
20 as to make it half open. Thus, a solid-state image pickup device according to the invention does not need to comprise a vertical type overflow drain that can be prepared only with difficulty nor a horizontal type overflow drain that obstructs the effort of reducing
25 the pixel size. Therefore, a solid-state image pickup device according to the invention is particularly adapted to reducing the pixel size.

Additionally, a solid-state image pickup device according to the invention is adapted to carry out a so-called rolling shutter operation by resetting the photodiodes by means of the transfer switch after
5 reading the signals to the floating diffusion region on a row by row basis.

Still additionally, the photodiode of any selected pixel can be reset by arranging a decoder in the scanning section of the control electrode of the
10 transfer switch.

On the other hand, the transfer switch can be opened for all the pixels by holding the floating diffusion region to a voltage level with which a reverse bias voltage higher than the depletion voltage
15 can be applied. With such an arrangement, the transfer switch can be used as the electronic shutter of an electric still camera.

As described above, according to the invention, since the transfer switch can be opened while holding
20 the floating diffusion region to a voltage level so that a reverse bias voltage higher than the depletion voltage can be applied, it is possible to carry out a resetting operation of depleting the photoelectric converter prior to the storage period. This means that
25 a greater tolerance is allowed for variances in designing and manufacturing solid-state image pickup images and hence the manufacturing yield will be

improved.

Finally, according to the invention, any residual
signal charge can be eliminated at the time of
resetting operation under a condition where all the
5 electric charge cannot be transferred in the reading
period.

WHAT IS CLAIMED IS:

1. A solid-state image pickup device comprising a photoelectric converter, an input terminal for a signal amplifier, a transfer switch for transferring an electric charge from the photoelectric converter to the input terminal and a reset switch for applying a reset voltage to the input terminal, wherein said device is adapted to input a pulse signal to the reset switch and the transfer switch in order to turn on said reset switch and said transfer switch simultaneously.

2. A solid-state image pickup device according to claim 1, wherein said reset voltage applied to the input terminal by means of said reset switch is selected to be higher than the depletion voltage defined as a reverse bias voltage sufficiently high for substantially depleting the semiconductor region of said photoelectric converter.

3. A solid-state image pickup device according to claim 1, wherein said photoelectric converter comprises a buried type photodiode.

4. A solid-state image pickup device according to claim 1, wherein said transfer switch is a switch for depletion-transferring the electric charge stored in said photoelectric converter.

5 5. A solid-state image pickup device according to
claim 1, wherein said transfer switch is a switch for
transferring the electric charge stored in said
photoelectric converter, leaving part of the electric
charge in said photoelectric converter.

10 6. A solid-state image pickup device according to
claim 1, wherein the reset voltage is so selected as to
make the potential energy of said input terminal lower
than the potential energy of said photoelectric
converter when said transfer switch and said reset
switch are on.

15 7. A solid-state image pickup device according to
claim 1, wherein said transfer switch is made half-open
to cause any excessive electric charge to flow to said
input terminal during the storage period of the device.

20 8. A solid-state image pickup device according to
claim 1, wherein the resetting operation of turning on
both said transfer switch and said reset switch is
conducted on a row by row basis for the photoelectric
converter.

25 9. A solid-state image pickup device according to
claim 1, wherein the resetting operation of turning on
both said transfer switch and said reset switch is

conducted at once for all the rows.

10. A solid-state image pickup device according to claim 1, wherein the resetting timing of turning on
5 both said transfer switch and said reset switch is modified depending on the quantity of light entering said photoelectric converter.

11. A solid-state image pickup device according
10 to claim 1, wherein said photoelectric converter, said input terminal for a signal amplifier and said transfer switch are arranged on a same semiconductor substrate.

12. A solid-state image pickup device according
15 to claim 1, wherein said input terminal is a diffusion region.

13. A solid-state image pickup device according to claim 1, wherein said photoelectric converter is a
20 photodiode comprising a first semiconductor region of a first conductivity type formed in a semiconductor substrate, a second semiconductor region of a second conductivity type located within said first semiconductor region and a third semiconductor region
25 of the first conductivity type located between said second semiconductor region and an insulation film formed on the principal surface of the semiconductor

substrate.

14. An image input apparatus comprising:
a solid-state image pickup device as defined in
5 claim 1; and

a mechanical shutter for defining the exposure
time of the solid-state image pickup device.

15. An image input apparatus according to claim
10 14, wherein the photoelectric charge storage period is
defined by the resetting operation of said solid-state
image pickup device and the opening/closing operation
of said mechanical shutter.

15 16. A method of resetting a solid-state image
pickup device as defined in claim 1, comprising a step
of turning on said reset switch and said transfer
switch simultaneously, before storing an electric
charge, to eliminate an electric charge of said
20 photoelectric converter.

17. A solid-state image pickup device comprising
a photoelectric converter, an input terminal for a
signal amplifier, a transfer switch for transferring an
25 electric charge from the photoelectric converter to the
input terminal, a reset switch for applying a reset
voltage to the input terminal and a circuit for

generating a pulse signal in order to turn on said reset switch and said transfer switch simultaneously.

18. A solid-state image pickup device according
5 to claim 17, wherein said reset voltage applied to the input terminal by means of said reset switch is selected to be higher than the depletion voltage defined as a reverse bias voltage sufficiently high for substantially depleting the semiconductor region of
10 said photoelectric converter.

19. A solid-state image pickup device according
to claim 17, wherein said photoelectric converter comprises a buried type photodiode.
15

20. A solid-state image pickup device according
to claim 17, wherein said transfer switch is a switch for depletion-transferring the electric charge stored in said photoelectric converter.
20

21. A solid-state image pickup device according
to claim 17, wherein said transfer switch is a switch for transferring the electric charge stored in said photoelectric converter, leaving part of the electric
25 charge in said photoelectric converter.

22. A solid-state image pickup device according

to claim 17, wherein the reset voltage is so selected
as to make the potential energy of said input terminal
lower than the potential energy of said photoelectric
converter when said transfer switch and said reset
5 switch are on.

23. A solid-state image pickup device according
to claim 17, wherein said transfer switch is made half-
open to cause any excessive electric charge to flow to
10 said input terminal during the storage period of the
device.

24. A solid-state image pickup device according
to claim 17, wherein the resetting operation of turning
15 on both said transfer switch and said reset switch is
conducted on a row by row basis for the photoelectric
converter.

25. A solid-state image pickup device according
20 to claim 17, wherein the resetting operation of
turning on both said transfer switch and said reset
switch is conducted at once for all the rows.

26. A solid-state image pickup device according
25 to claim 17, wherein the resetting timing of turning on
both said transfer switch and said reset switch is
modified depending on the quantity of light entering

said photoelectric converter.

27. A solid-state image pickup device according
to claim 17, wherein said photoelectric converter, said
5 input terminal for a signal amplifier and said transfer
switch are arranged on a same semiconductor substrate.

28. A solid-state image pickup device according
to claim 17, wherein said input terminal is a diffusion
10 region.

29. A solid-state image pickup device according
to claim 17, wherein said photoelectric converter is a
photodiode comprising a first semiconductor region of a
15 first conductivity type formed in a semiconductor
substrate, a second semiconductor region of a second
conductivity type located within said first
semiconductor region and a third semiconductor region
of the first conductivity type located between said
20 second semiconductor region and an insulation film
formed on the principal surface of the semiconductor
substrate.

30. An image input apparatus comprising:
25 a solid-state image pickup device as defined in
claim 17; and
a mechanical shutter for defining the exposure

time of the solid-state image pickup device.

31. An image input apparatus according to claim
30, wherein the photoelectric charge storage period is
5 defined by the resetting operation of said solid-state
image pickup device and the opening/closing operation
of said mechanical shutter.

32. A method of resetting a solid-state image
10 pickup device as defined in claim 17, comprising a step
of turning on said reset switch and said transfer
switch before storing an electric charge to eliminate
the electric charge of said photoelectric converter.

ABSTRACT OF THE DISCLOSURE

A solid-state image pickup device comprises for each pixel a photoelectric converter PD, an input terminal FD of a signal amplifier and a transfer switch TX for transferring an optical signal from the photoelectric converter to the input terminal. The device additionally comprises means for resetting the photoelectric converter by opening the transfer switch TX under a condition of holding the voltage of the input terminal FD to a fixed high level before storing the optical signal in the photoelectric converter PD. With this arrangement, any residual electric charge in the photoelectric converter can be eliminated without paying the cost of reducing the manufacturing yield and degrading the chip performance.

FIG. 1

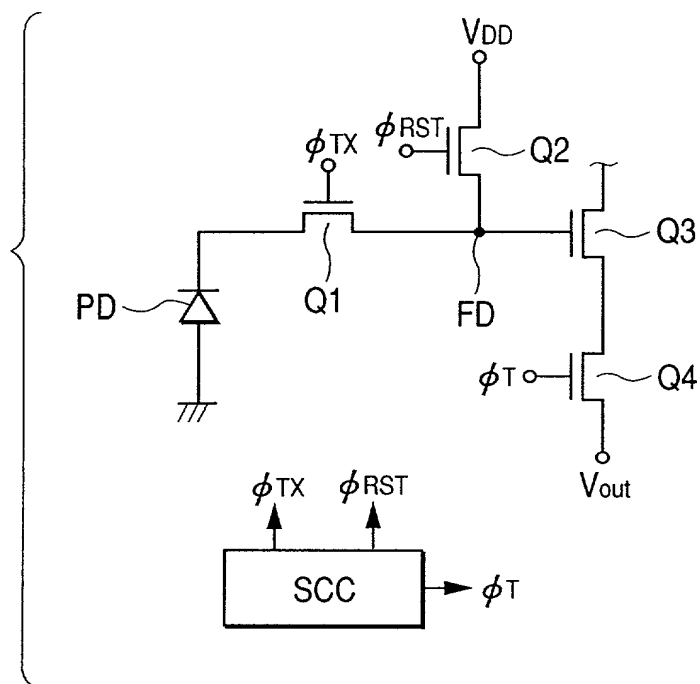


FIG. 3

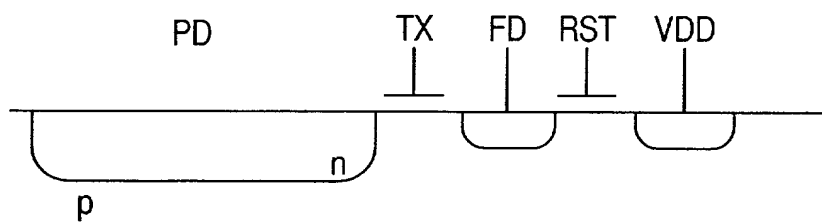


FIG. 2

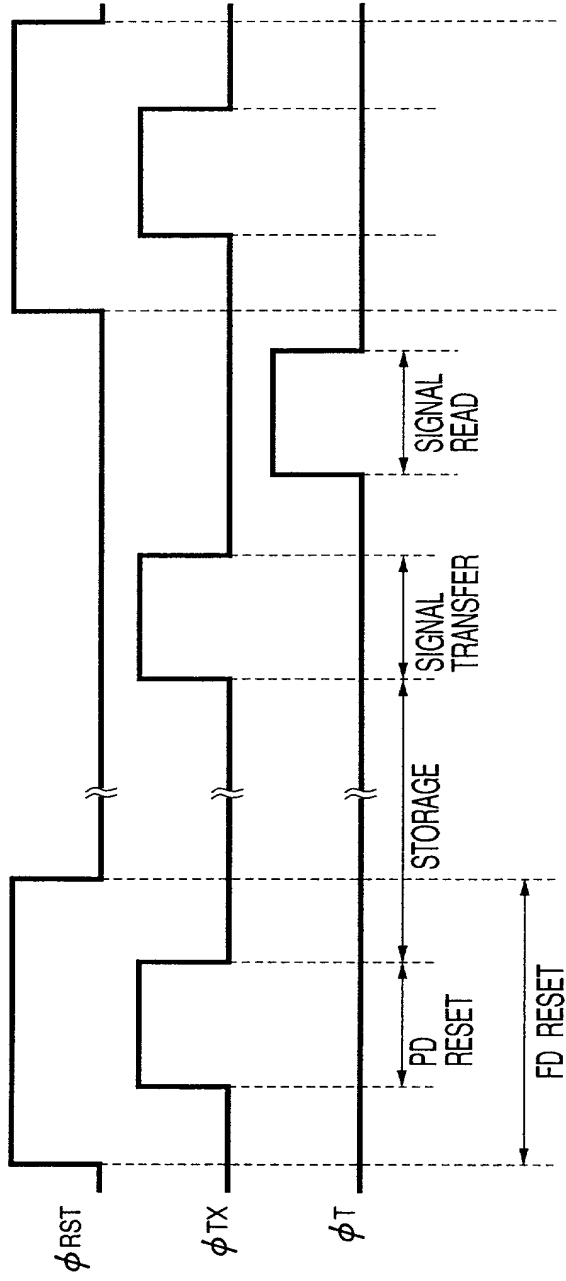


FIG. 4

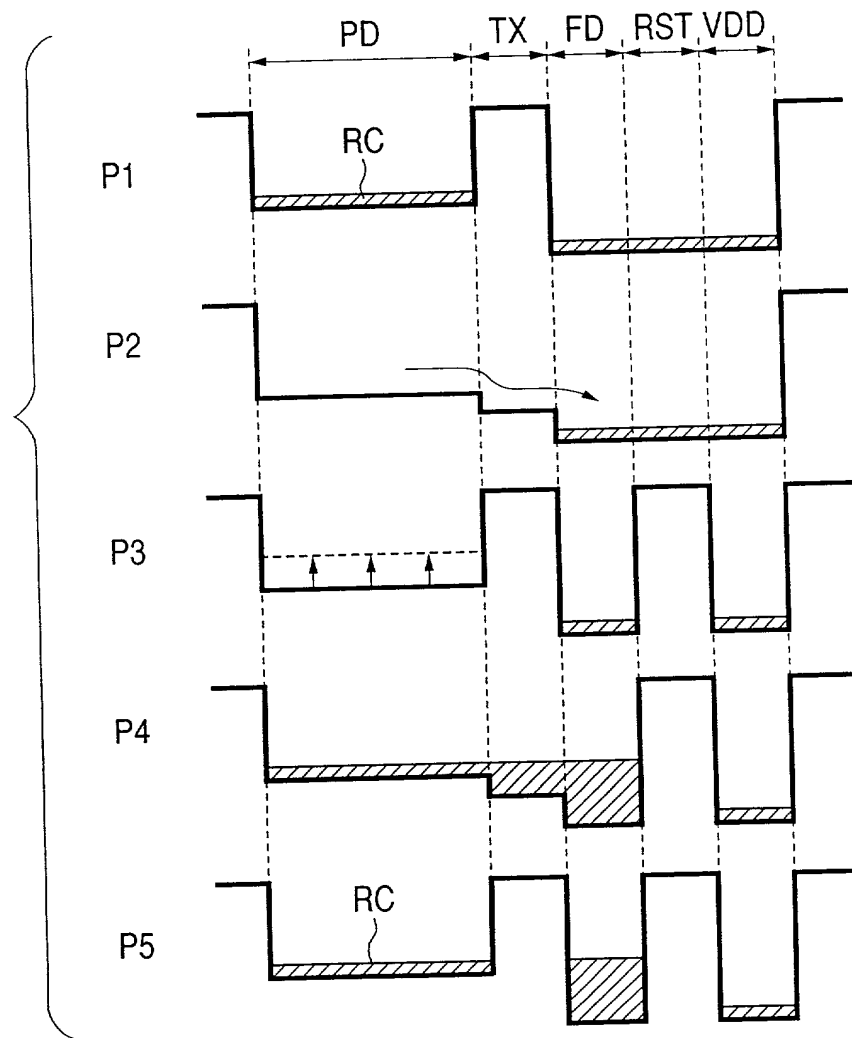


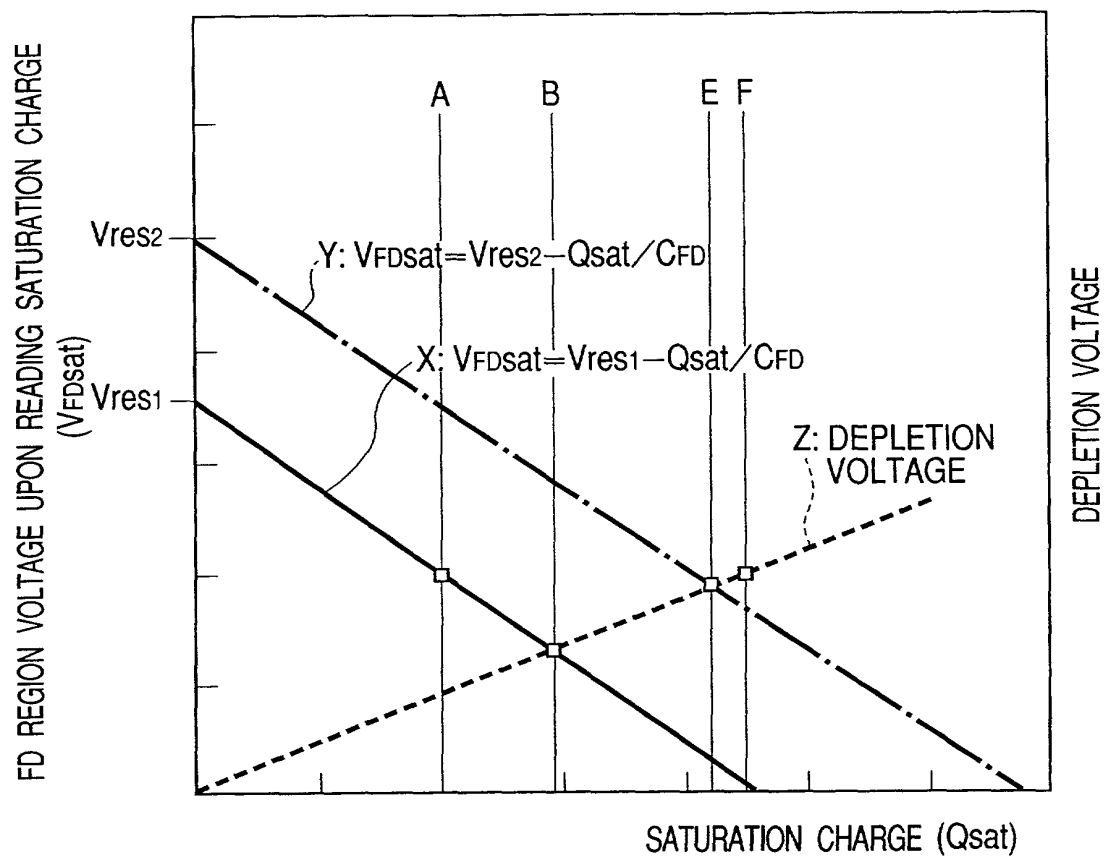
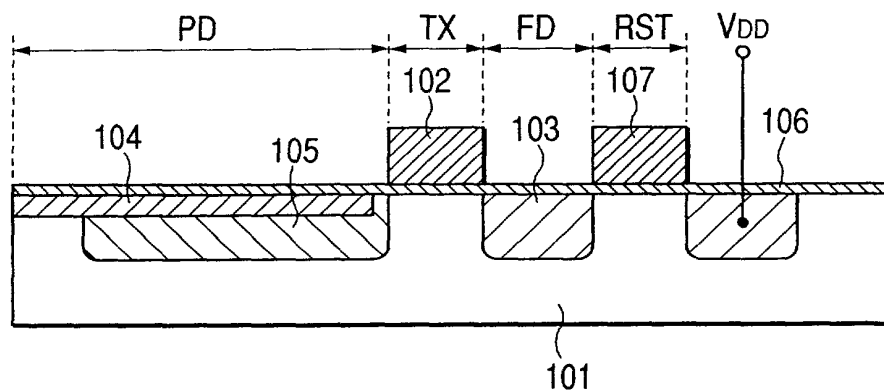
FIG. 5**FIG. 6**

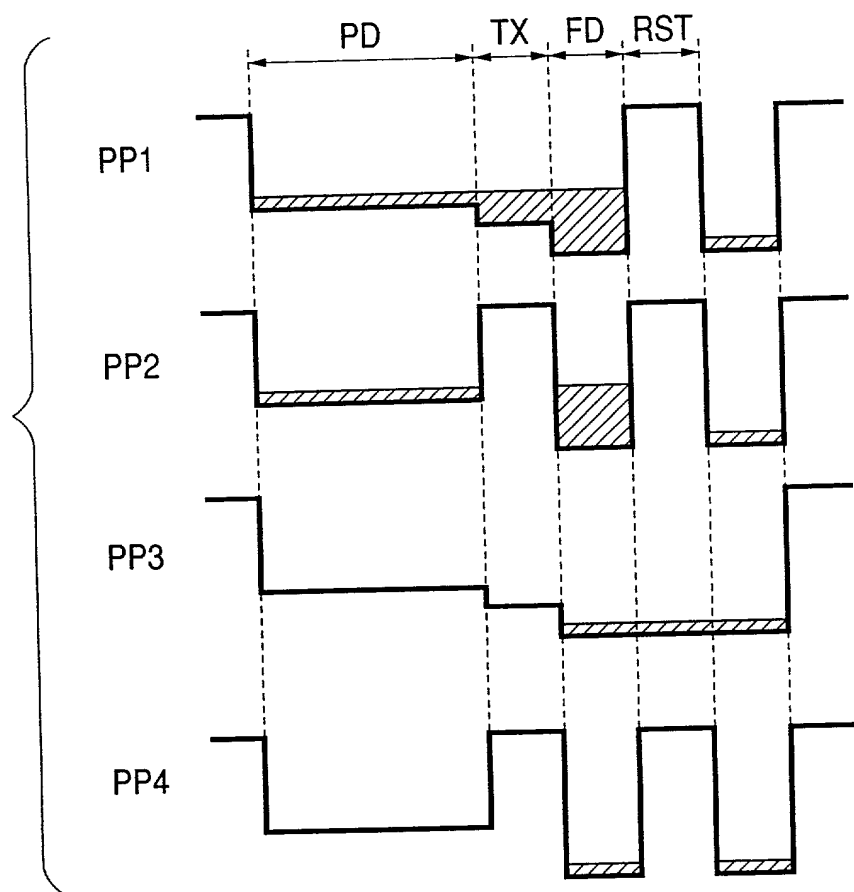
FIG. 7

FIG. 10

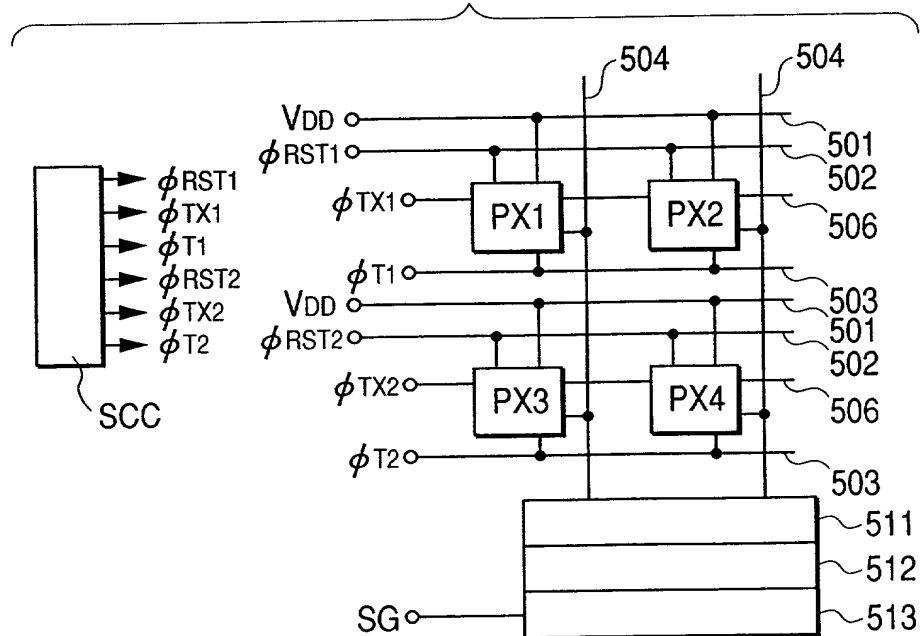


FIG. 11

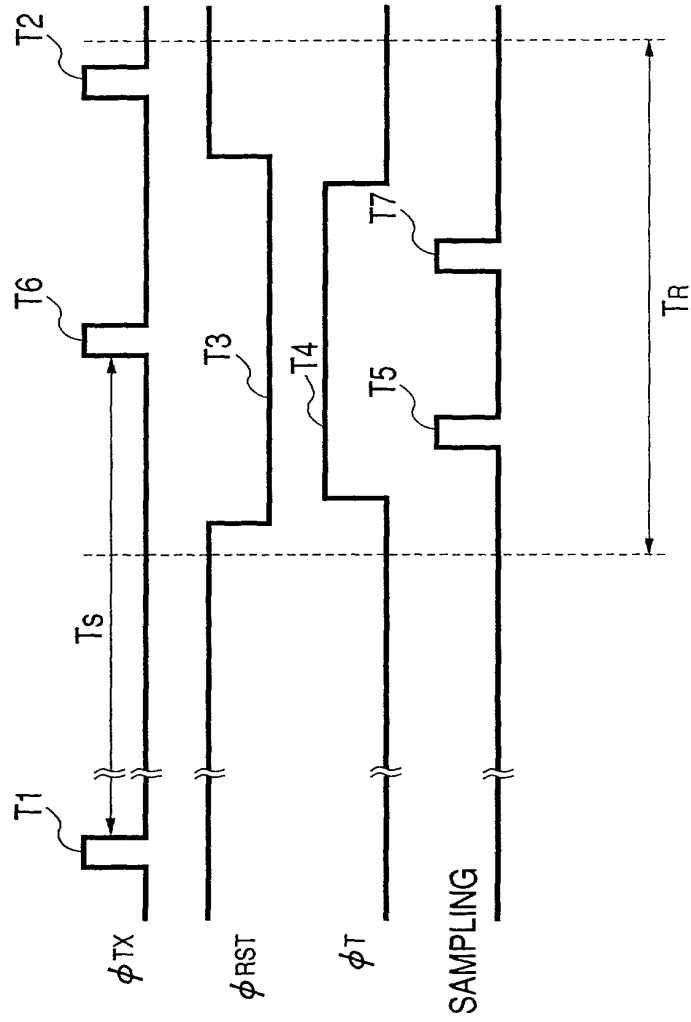


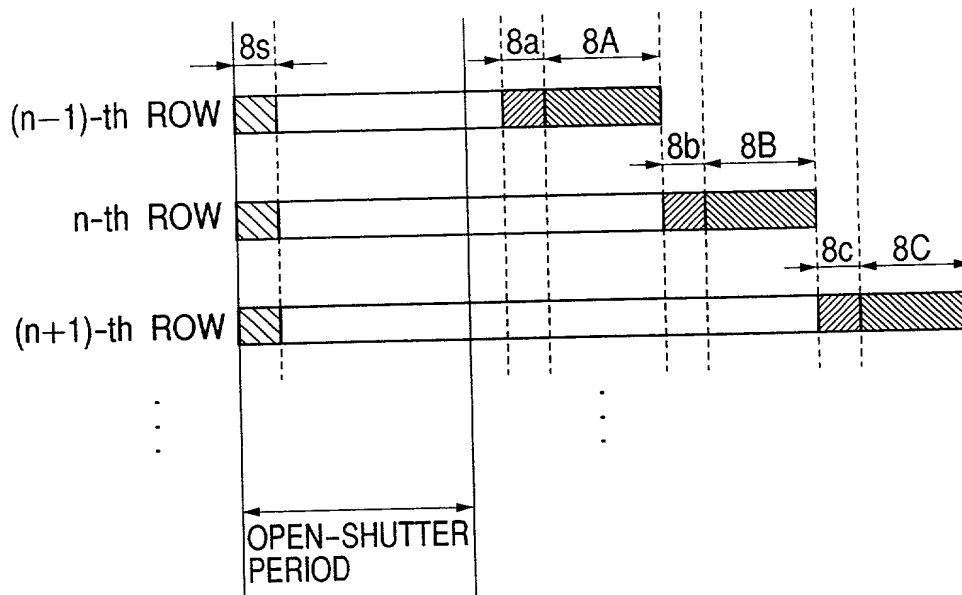
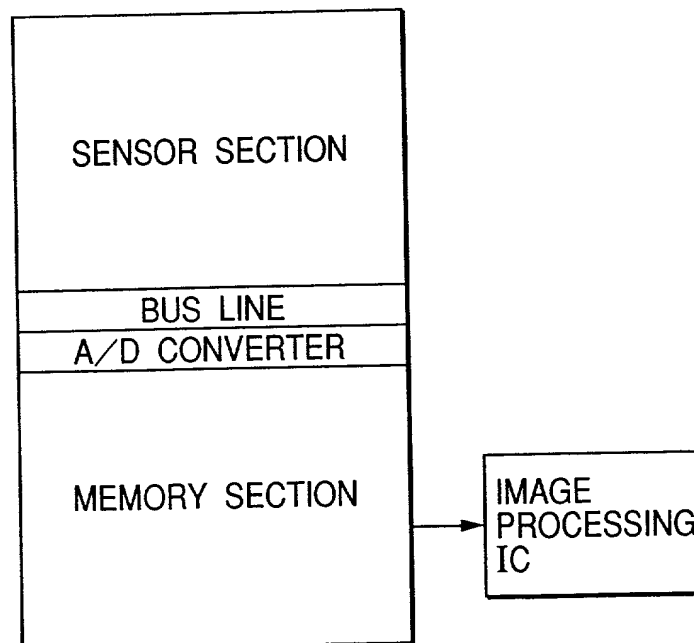
FIG. 14**FIG. 15**

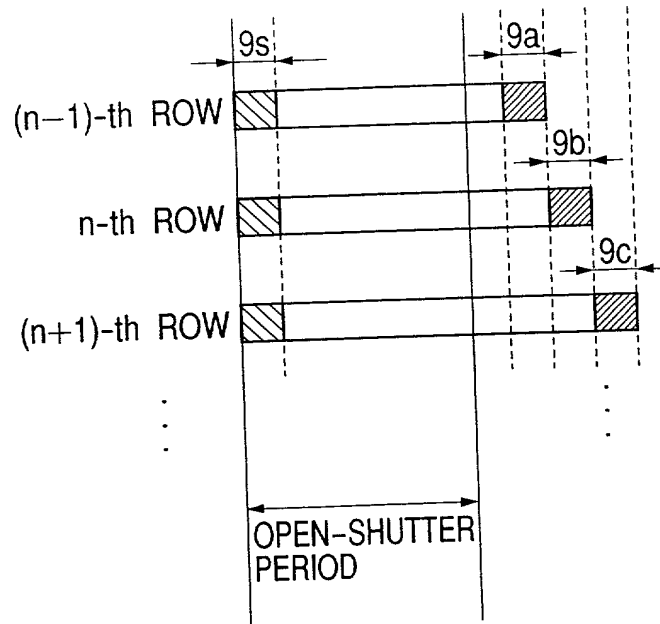
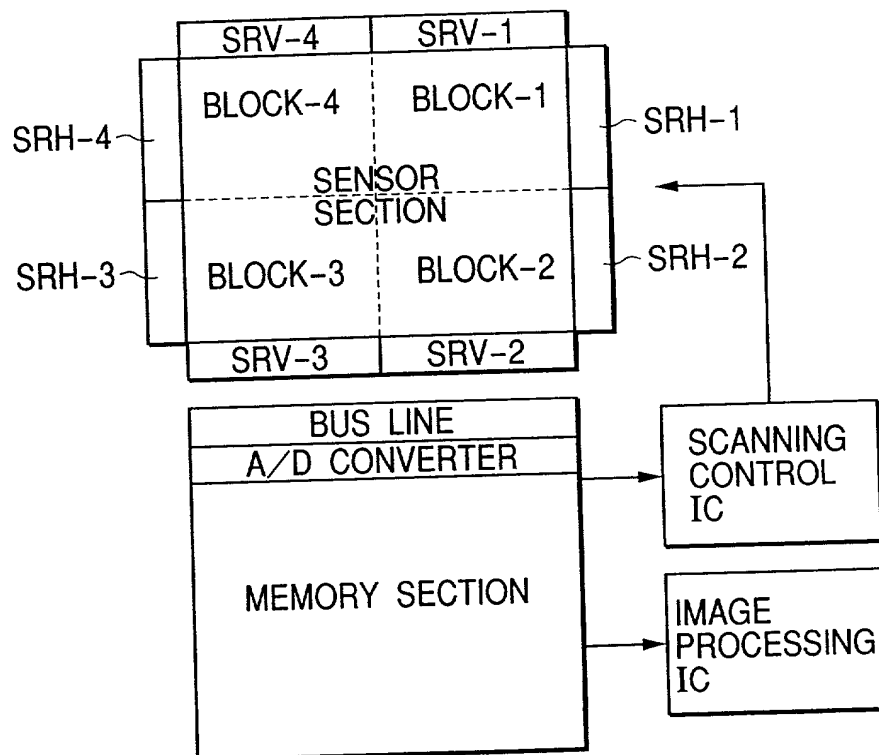
FIG. 16**FIG. 17**

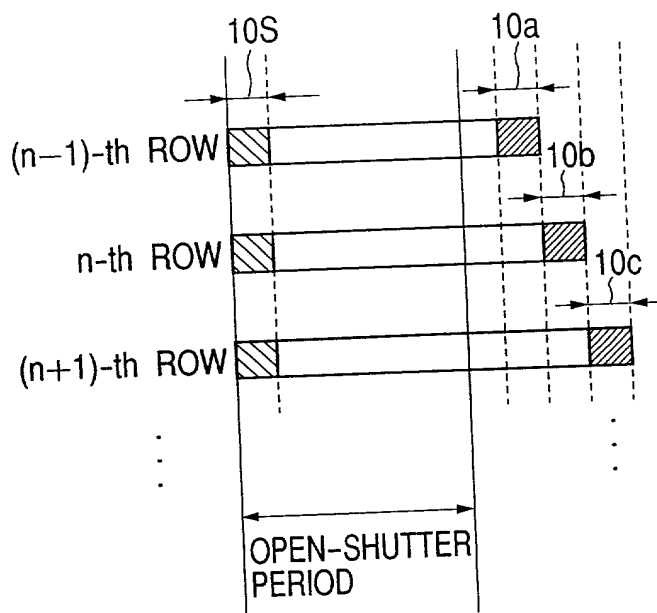
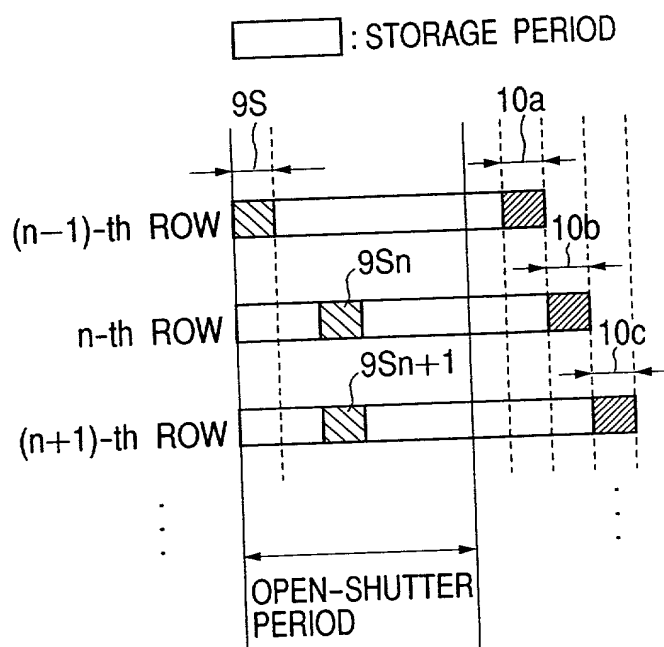
FIG. 18**FIG. 19**

FIG. 20

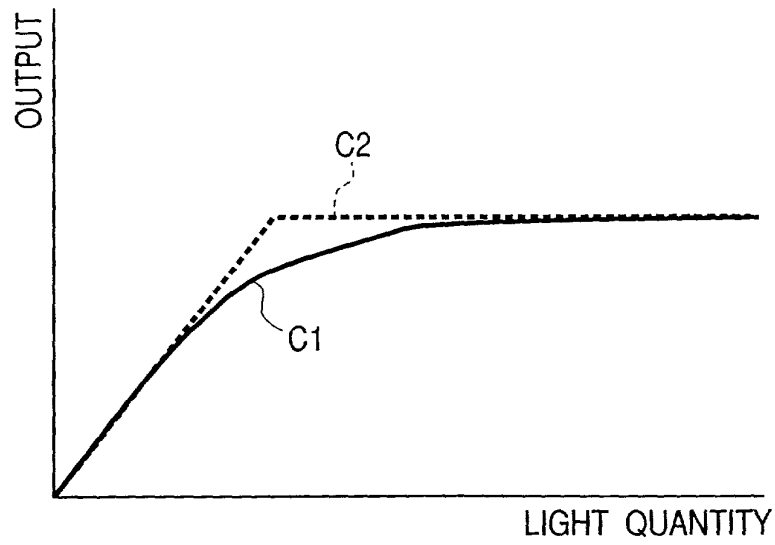


FIG. 21

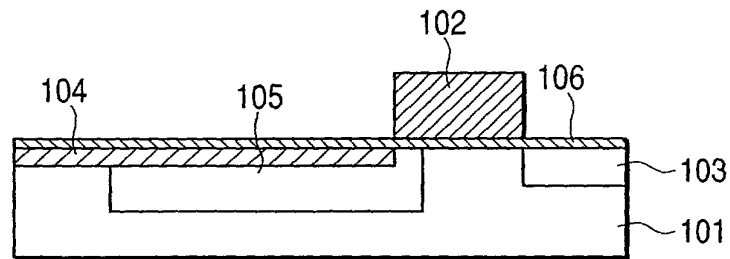


FIG. 22

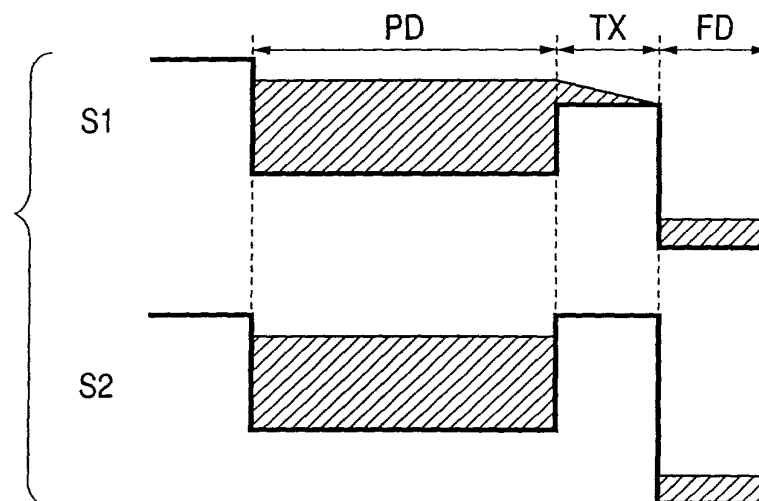


FIG. 23

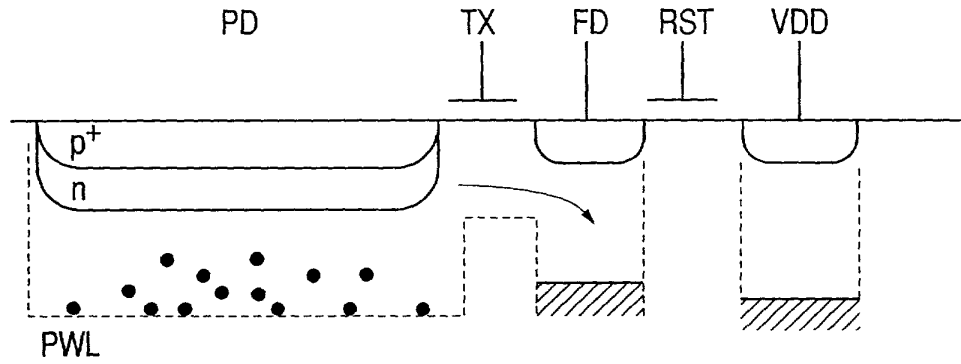
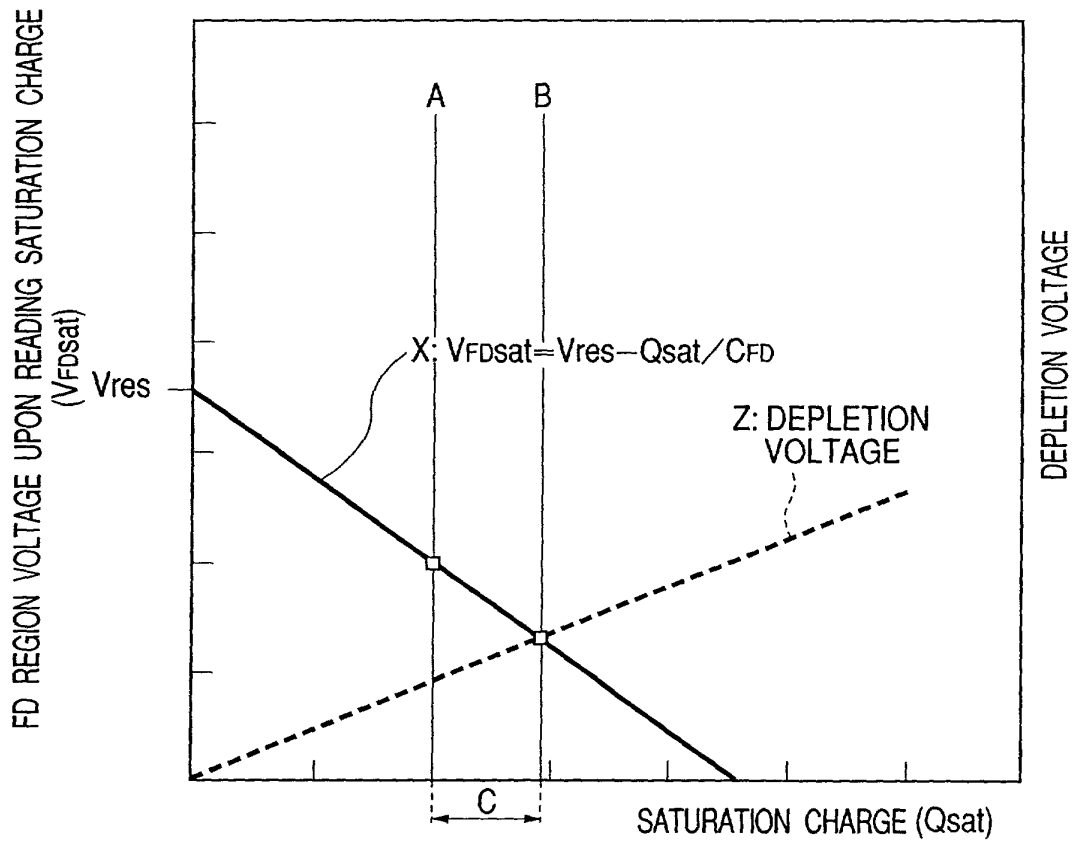


FIG. 24



**COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION**
(Page 1)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled SOLID-STATE IMAGE PICKUP DEVICE AND METHOD OF RESETTNG THE SAME

the specification of which ☒ is attached hereto ☐ was filed on _____ as United States Application No. or PCT International Application No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or §365(b), of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designates at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed:

<u>Country</u>	<u>Application No.</u>	<u>Filed (Day/Mo./Yr.)</u>	<u>(Yes/No)</u> <u>Priority Claimed</u>
Japan	10-312281	November 2, 1998	Yes

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

<u>Application No.</u>	<u>Filed (Day/Mo./Yr.)</u>	<u>Status</u> <u>(Patented, Pending, Abandoned)</u>
------------------------	----------------------------	--

I hereby appoint the practitioners associated with the firm and Customer Number provided below to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to the address associated with that Customer Number.

FITZPATRICK, CELLA, HARPER & SCINTO
Customer Number: 05514

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature _____

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COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION

(Page 2)

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Fourth Inventor's signature _____

Date _____ Citizen/Subject of _____

Residence _____

Post Office Address _____

Full Name of Fifth Joint Inventor, if any _____

Fifth Inventor's signature _____

Date _____ Citizen/Subject of _____

Residence _____

Post Office Address _____

Full Name of Sixth Joint Inventor, if any _____

Sixth Inventor's signature _____

Date _____ Citizen/Subject of _____

Residence _____

Post Office Address _____

Full Name of Seventh Joint Inventor, if any _____

Seventh Inventor's signature _____

Date _____ Citizen/Subject of _____

Residence _____

Post Office Address _____